Design of Video Interface Conversion System based on FPGA

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ABSTRACT

This paper presents a FPGA based video interface conversion system that enables the inter-conversion between digital and analog video. Cyclone IV series EP4CE22F17C chip from Altera Corporation is used as the main video processing chip, and single-chip is used as the information interaction control unit between FPGA and PC. The system is able to encode/decode messages from the PC. Technologies including video decoding/encoding circuits, bus communication protocol, data stream de-interleaving and de-interlacing, color space conversion and the Camera Link timing generator module of FPGA are introduced. The system converts Composite Video Broadcast Signal (CVBS) from the CCD camera into Low Voltage Differential Signaling (LVDS), which will be collected by the video processing unit with Camera Link interface. The processed video signals will then be inputted to system output board and displayed on the monitor.The current experiment shows that it can achieve high-quality video conversion with minimum board size.

Keywords: FPGA, ITU-R BT.656, Camera Link, Video Conversion, Color Space

1. INTRODUCTION

With the rapid development of multimedia, digital communications technology, a variety of image acquisitions and display products abound. However, because the device interface standards are highly inconsistent, the interconnection issue between different devices, in particular between digital and analog connectors, has becoming increasingly prominent. Currently, the majority connector of the image capture cards is Camera Link, which cannot directly obtain the data from an analog output interface. Therefore, it is desirable to design a device that could enable the inter-conversion between analog and digital video interface.[1–3]

With the inherent advantages of low voltage, low power consumption, conducive to high-speed transmission and other characteristics, Camera Link technology is gradually becoming the preferred interface of high-speed systems. Camera Link has wide applications in the field of communications.[4]

This paper gives a solution for the conversion between BNC interface and Camera Link interface without adding any external memory, it achieves all the requirements of a practical project within a strict limit on board size that no more than 110mm*70mm.

2. ARCHITECTURE OF VIDEO CONVERSION SYSTEM

The system consists of two parts, the input and output boards. Input board receives the analog video from the CCD camera through BNC port, and then it converts analog video into digital signals by video decoder chip. Afterwards, the digital signal is inputted into FPGA for data stream de-interweaving, de-interlacing, color space conversion and the Camera Link timing generating. FPGA eventually converts the digital signal into the video signal that complies with the Camera Link protocol and inputs it to the video capture card.

The output board receives the processed signal from the video capture card. The Channel Link receiver then converts the signal from the Camera Link port into signal that can be processed by the core processer. After

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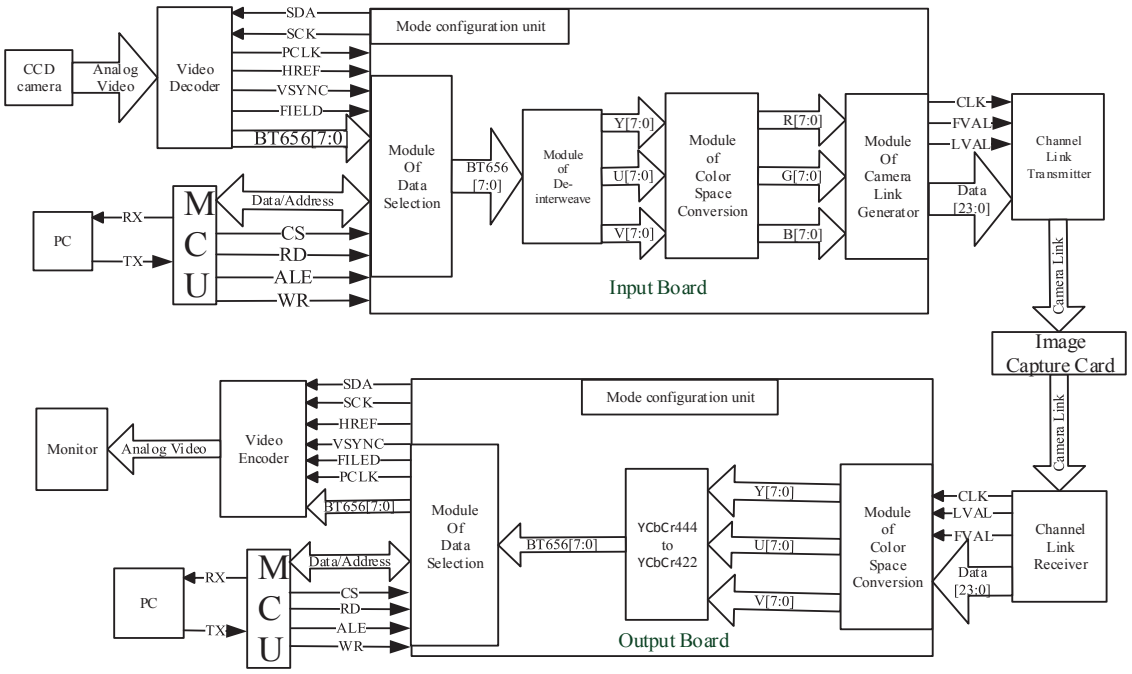

Figure 1. Diagram of Video Conversion System

color space conversion the signal is outputted to the video encoder chip and displayed on a monitor through a BNC video port. Diagram of video conversion system is shown in Fig 1.

In the input board, the video decoder circuits convert the analog video into a 8-bit parallel digital signal in ITU-R BT.656 format, a 27 MHz clock signal and the horizontal and vertical sync signals. Each pixel value of YCbCr in the data stream is interleaved together in a serial and therefore needs to be de-interleaved before the conversion. Since the original form of the video signal is interlaced in odd and even alternating field, while the Camera Link protocol is progressive scanning, de-interlacing module is needed to store the data and accomplish the conversion of video display from interlaced scanning to progressive scanning. Moreover, as Capture card compatible to this system requires the input in RGB tricolor synthesis, whereas the color space of the data from video decoder chip is YCbCr, the color space conversion from YCbCr to RGB is necessary.Camera Link timing generator module transmits the processed video data according to the Camera Link protocol. The LVDS data must be sent through the Camera Link interface; therefore the Channel Link transmitter has to convert the parallel TTL/COMS signals into LVDS data streams. MCU transfers data from PC to FPGA and replaces the target position data simultaneously with video transmission.

The output board receives the data that has been processed by image capture card through the Camera Link interface. Next, the Channel Link receiver converts the LVDS into 28-bit TTL/COMS signals. As the video encoder chip supports only 8/16 YCrCb4:2:2 format signal input, RGB color space to the YCrCb andYCrCb4:4:4 to YCrCb4:2:2 conversions are required.

3. HARDWARE IMPLEMENTATION

Diagrams of hardware structure of the system is shown in Fig 2 and Fig 3. It includes several modules as shown in below.

3.1 Video Decoder/Encoder Circuits

The system video decoder chip is ADV7181B from Analog Device, which can automatically detect and transform standard NTSC/PAL analog TV baseband composite signal to 4:2:2-standard composite CCIR601/CCIR656 16/8 composite video data. Particularly, it supports 6-channels analog video input.

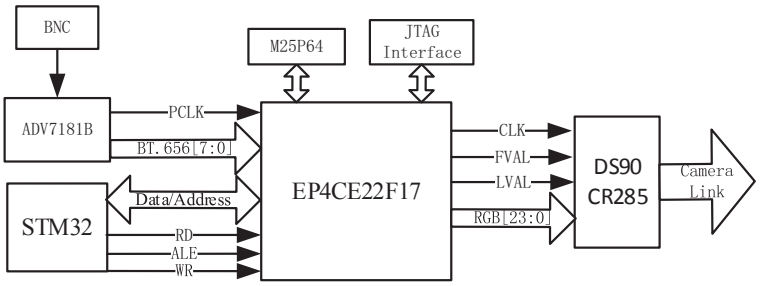

Figure 2. Hardware Structure of System Input Board

ADV7171 from Analog Device is chosen as the system video encoder chip, which can encode the digital video signal into NSTC/PAL format signal that can be received by a regular television.

3.2 Interface Circuit of Camera Link

In this circuit, we use LVDS transmitter DS90CR285 and receiver DS90CR286 from National Semiconductor to accomplish the voltage conversion between LVDS and TTL/COMS. The Channel Link transmitter converts 28-bit of TTL/COMS data into four LVDS data streams and a PLL clock signal through the fifth pair of LVDS link. The Channel Link receiver converts the data stream back into 28-bit of TTL/COMS data and a received clock signal.

3.3 Module of Power Supply

Due to the constraints in the practical environment, power supply of the system is 12V. However the majority operating voltage of chips is 3.3V. FPGA has specification for the core and auxiliary voltage rails, respectively 1.2V and 2.5V.In addition, 1.8V power supply is required for ADV7181B.Therefore, voltage regulator chips to convert 12V to 3.3V and 3.3V to 1.2V, 1.8V, 2.5V are needed. To meet the power requirements, regulator chip should be used to provide proper power supplies for all chips. LT1765 is used to convert 12V to 3.3V, and AMS1117 to achieve 3.3V to 1.2V, 1.8V, and 2.5V in the system.

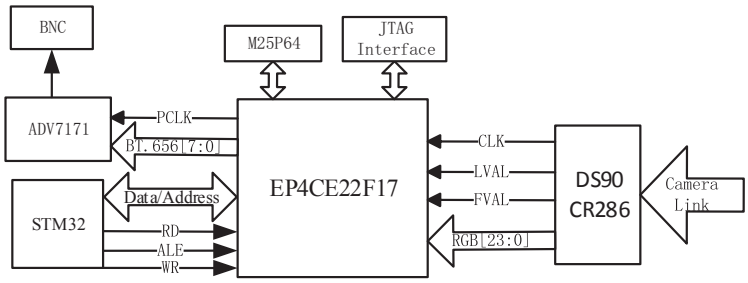

Figure 3. Hardware Structure of System Output Board

3.4 Communication Module of MCU

STM32F103 is selected as the system MCU to receive the data from PC using serial ports. It communicates messages with FPGA according to its own communication protocol through bus communication. Bus communication timing diagram between MCU and FPGA is shown in Fig 4.

As is shown in the diagram in Figure 4, CS is the chip select signal, ALE is the address lock enable signal, WR is the write enable signal, and RD is the read enable signal. After the read/write cycle begins, MCU sends 8-bit data/address wire to DataBus ports, and then the negative edge of the ALE will lock the address. MCU reads/writes data at the positive edge of the WR/RD signals.

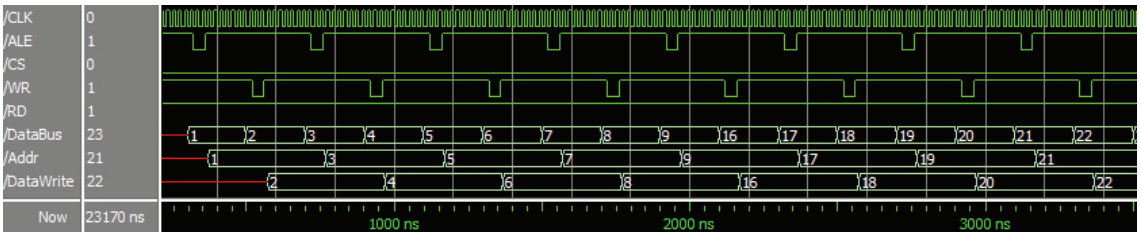

Figure 4. Communication Timing Diagram of MCU

3.5 Minimum System and Configuration Circuit of FPGA

As the timing control center and data exchange bridge of the system, FPGA is required to have rich internal resources. With internal resources, cost, chip size, secondary development of the system and other factors taken into consideration, Cyclone IV series EP4CE22F17C from Altera Corporation is the optimal choice. FPGA configuration mode uses the SPI serial Flash, and the flash chip selects the M25P64 from Numonyx. JTAG configuration mode is set in order to facilitate debugging.

4. MODULE DESIGN IN FPGA

4.1 Communication Module of I^2C Bus

There are a number of internal control registers that can be configured to implement various functions of ADV7181B and ADV7171. Timing in accordance with the I2C bus is required for the data configuration of video decoder/encoder chips. As is shown in Fig 5, after FPGA resetting the global reset signal rst, signal data reads the register configuration data and starts data communication. Each communication cycle has 27 clock cycles; signal sda writes one data when the clock pulls signal scl. After writing 8 bits data, I/O ports of FPGA are changed to a high impedance state at the ninth clock to wait the ADV7181B pulling the corresponding data line.

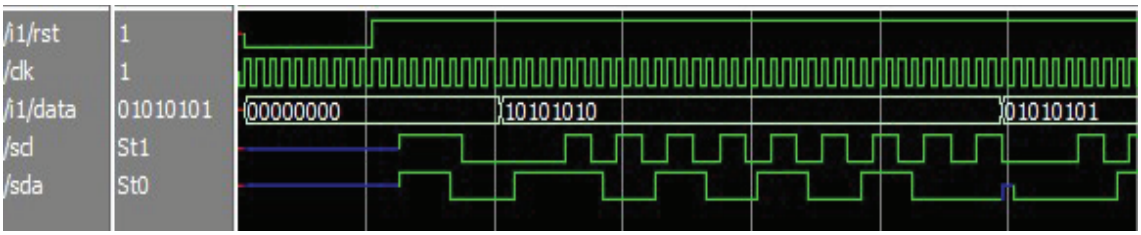

Figure 5. Timing Diagram of I^2C Configuration Register

4.2 Module of Data Stream Selection

The main function of this module is to encode the message from PC into video stream in ITU-R BT.656 format. In the process Y component in every frame is replaced, starting from the first effective pixel in the first line. The number of data to be replaced can be set according to specific needs. The Timing Diagram of data stream selection is shown in Fig 6.

Signal PCLK is the pixel clock; signal AD_DATA is the data stream in ITU-R BT.656 format; signal RAM_IN stores the messages that comes from PC and signal OUT is the data stream that will be received by the Module of De-interleaving.

4.3 Module of De-interleaving

Video decoder converts the analog video into digital video in ITU-R BT.656 format. Besides 4:2:2 YCbCr format video data, the ITU-R BT.656 parallel interface transmit horizontal and vertical synchronization control signals.

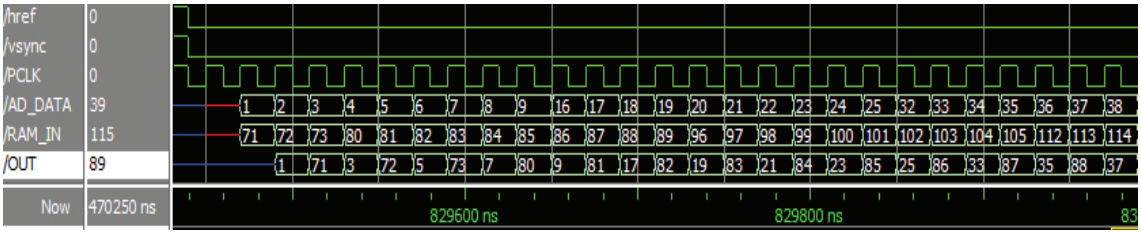

Figure 6. Timing Diagram of Data Stream Selection

An image frame is a data block composed of 625 lines, 1728 bytes for each line. Line 23 to 311 are even fields and line 366 to 624 are odd fields; the rest are vertical control signals.

There are two steps in a de-interleaving module. Firstly, de-interleaving module detects the start and end positions of a complete image data stream based on vertical sync signal from the video decoder chip; then the module interleaves the ITU-R BT.656 format data stream during the active period of the horizontal synchronization signal.

In the process of de-interleaving, each Cb, Cr is reused to separate each pixel of YCbCr. De-interleaving schematic process is shown in Fig 7:[5]

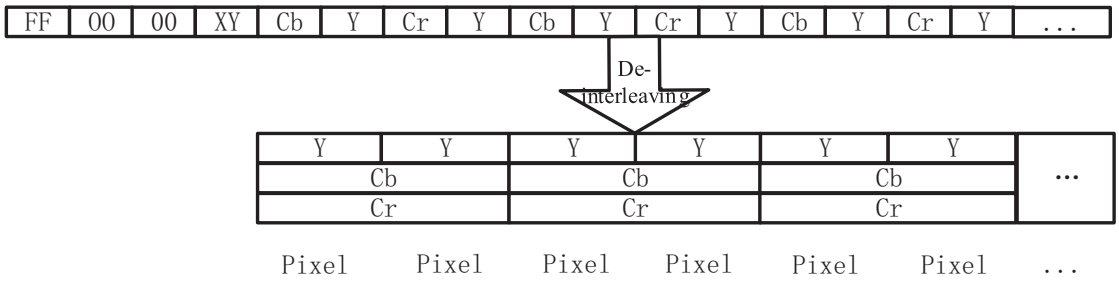

Figure 7. Diagram of De-interleaving

Fig 8 is the waveform simulation of the de-interleaving module. It takes 8 pixel clocks to convert the YCbCr4:2:2 data in YCbCr4:4:4 format, which fits the process in Fig 7.

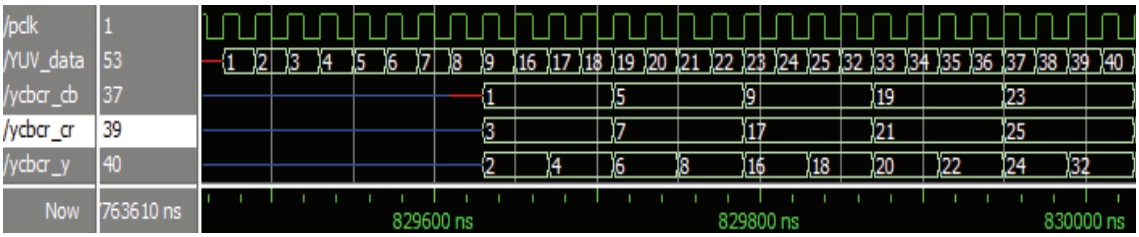

Figure 8. Timing Diagram of De-interleaving

4.4 Module of De-interlacing

De-interlacing is the process of converting interlaced video into a non-interlaced form. For the sake of cost and size reduction, the system uses the field line insertion method due to its lower memory requirements to achieve not adding SDRAM in the system.

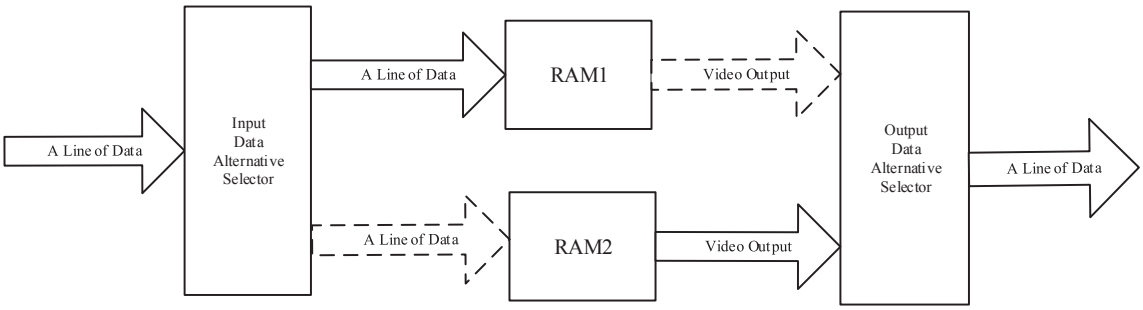

Figure 9. The procedure of Ping-pong operation

Field line insertion method converts interlaced scanning to progressive scanning. The on-chip RAM reuses the line image signal twice every time by writing data into the RAM at low speed and reading it at high speed. The process doubles the line frequency, while the field frequency remains unchanged. Field line insertion method uses three groups of logical memory and the corresponding switches to realize Ping-pong operation in FPGA. The procedure of Ping-pong operation is shown in Fig 9:

The module consists of six dual-port RAMs, six alternative selectors and read/write switch counters, in which the frequency of writing clock is 13.5MHz and reading clock is 27MHz. RAM is used to store the image data Y, Cb and Cr, respectively. Writing switch counter generates a writing strobe signal of RAM; Reading switch counter generates signals to read the data from two RAMs alternatively. Storing a row of data and reading the effective data twice simultaneously can replace the even lines with the odd line to achieve the progressive scanning.

4.5 Module of Color Space Conversion

The function of the YCbCr to RGB module is to convert the YCbCr values based on the effective signals from the de-interleaving module into corresponding RGB values. In experiment environment, the color space conversion formula between RGB and YCbCr is shown in equation (1).

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.402 \\ 1 & -0.344 & -0.714 \\ 1 & 1.772 & 0 \end{bmatrix} \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -179.456 \\ 135.424 \\ 226.816 \end{bmatrix} \tag{1}$$

As the floating-point arithmetic in the FPGA is difficult, coefficients transformation is needed in Equation (1). The rounding method is to enlarge the individual coefficient by 1024 times and divide the result of R, G and B by 1024, as is shown in Equation (2):[6–8]

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} \times 1024 = \begin{bmatrix} 1024 & 0 & 1436 \\ 1024 & -354 & -741 \\ 1024 & 1815 & 0 \end{bmatrix} \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -183763 \\ 138674 \\ 232260 \end{bmatrix} \tag{2}$$

Fig 10 shows the simulation waveforms of YCbCr to RGB. signal pclk is the clock signals; Y[7:0]Cb[7:0]Cr[7:0] are input signals; R[7:0]G[7:0]B[7:0] are output signals.

The width of the R, G, B signals are 8-bit with the rounding range from 0 to 255, while there can be minus numbers and positive numbers higher than 255 in the operation process. When displaying the results, numbers higher than 255 will be taken as 255, and minus will be taken as 0. This operation can introduce certain deviation, but it does not affect the display of the image. The RGB to YCbCr module in the output board is similar to the YCbCr to RGB module.

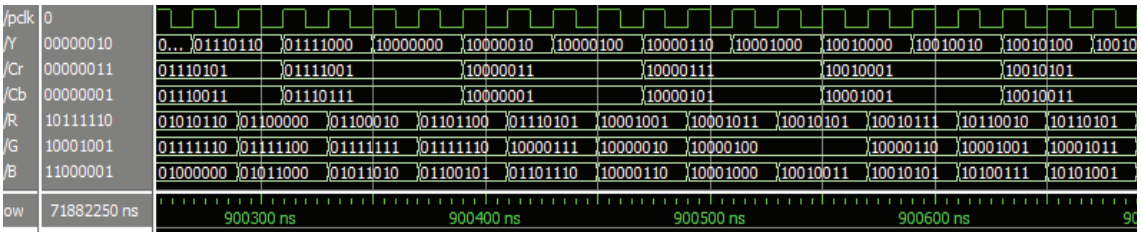

Figure 10. Simulation waveforms of YCbCr to RGB

4.6 Module of Camera Link Timing Generator

Timing of signal transmission according to Camera Link protocol is shown in Fig 11. LVAL is the line valid signal, whose high level state means outputting an effective pixel row; FVAL is the frame valid signal, whose high level state means outputting an effective pixel frame; DVAL is the data valid signal which will be high when FVAL and LVAL are high. It means outputting valid data. CLK and DATA respectively represent pixel clock and effective video data.[9, 10]

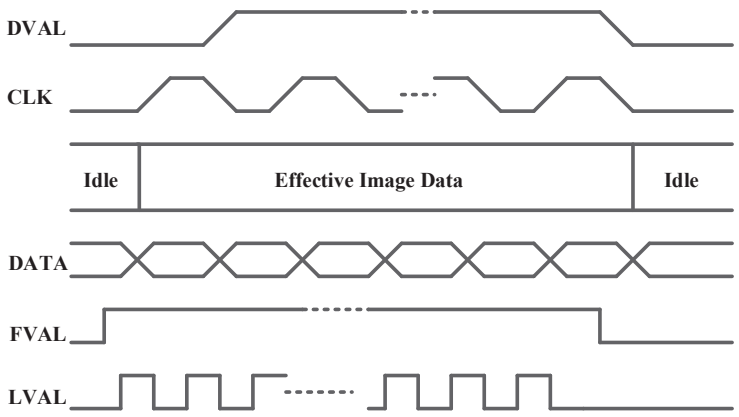

Figure 11. Diagram of signal transmission under Camera Link protocol

According to the definition, DVAL has no effect on the output. Only FVAL and LVAL are used in the design. When FVAL and LVAL are high, CLK controls to send DATA in turn.

Under the control of the CLK, Camera Link timing generator assigns 24-bit image data, frame valid signal and line valid signal according to the definition of the Camera Link interface. It converts the TTL/COMS into LVDS data stream by the level conversion chip.

5. CONCLUSION

With the application of field programmable chip FPGA, advantages such as flexibility and high integration are reflected in the design. It enables the inter-conversion between the BNC and Camera Link interface and achieves the de-interlacing process by simple storage control. The design avoids complex internal algorithm process in FPGA and achieves high-quality video conversion with fewer hardware resource in FPGA, which proves to possess good engineering practicality.

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